

WHAT IS CLAIMED IS:

- 1 1. A serial stream interface for combining a master serial data stream comprising a sequence of N-bit master data packets and a slave serial data stream comprising a sequence of N-bit slave data packets, said serial stream interface comprising:
 - 5 a slave input interface comprising a slave buffer having a serial input for receiving said slave serial data stream and an N-bit slave parallel output for outputting each of said N-bit slave data packets, wherein said slave buffer stores said each N-bit slave data packet using at least one slave timing signal associated with said slave serial data stream;
 - 11 a source selection circuit having a first input channel capable of receiving an N-bit master parallel output from a first master data source and a second input channel coupled to said N-bit slave parallel output; and
 - 15 a serialization circuit having an input coupled to an output of said source selection circuit capable of receiving a selected one of said N-bit master parallel output and said N-bit slave parallel output and a serial output, wherein said serialization circuit sequentially shifts out each bit of said selected one of said N-bit master parallel output and said N-bit slave parallel output to produce an output serial data stream.

1 2. The serial stream interface as set forth in Claim 1
2 wherein each bit in said each N-bit slave data packet stored in
3 said slave buffer becomes available in said N-bit slave parallel
4 output substantially concurrently with storage of said each bit in
5 said slave buffer.

1 3. The serial stream interface as set forth in Claim 2
2 wherein said slave buffer is a first-in, first-out (FIFO) device.

1 4. The serial stream interface as set forth in Claim 3
2 wherein said slave buffer is a 1xN-bit random access memory (RAM).

1 5. The serial stream interface as set forth in Claim 1
2 wherein said slave input interface further comprises a slave
3 control circuit capable of receiving said at least one slave timing
4 signal and generating therefrom at least one storage control signal
5 capable of storing said each of said N-bit slave data packets in
6 said slave buffer.

1 6. The serial stream interface as set forth in Claim 1
2 wherein said source selection circuit comprises a first multiplexer
3 having an M-bit output.

1 7. The serial stream interface as set forth in Claim 6
2 wherein said serialization circuit comprises a second multiplexer
3 having a first M-bit input channel coupled to said M-bit output of
4 said first multiplexer.

1 8. The serial stream interface as set forth in Claim 7
2 wherein said serialization circuit comprises a flip-flop circuit
3 having an M-bit input coupled to an M-bit output of said second
4 multiplexer, wherein said flip-flop latches M-bits of data received
5 from said second multiplexer on an M-bit output of said flip-flop.

1 9. The serial stream interface as set forth in Claim 8
2 wherein said second multiplexer further comprises a second M-bit
3 input channel coupled to said M-bit output of said flip-flop.

1 10. A radio frequency (RF) receiver comprising:

2 a receiver front-end circuit capable of receiving an
3 incoming RF signal from an antenna and generating an amplified RF
4 output signal;

5 demodulation circuitry capable of demodulating said
6 amplified RF output signal and generating a plurality of baseband
7 serial data streams;

8 a serial stream interface capable of receiving said
9 plurality of baseband serial data streams and combining a master
10 serial data stream comprising a sequence of N-bit master data
11 packets and a slave serial data stream comprising a sequence of N-
12 bit slave data packets, said serial stream interface comprising:

13 a slave input interface comprising a slave buffer
14 having a serial input for receiving said slave serial data
15 stream and an N-bit slave parallel output for outputting each
16 of said N-bit slave data packets, wherein said slave buffer
17 stores said each N-bit slave data packet using at least one
18 slave timing signal associated with said slave serial data
19 stream;

20 a source selection circuit having a first input
21 channel capable of receiving an N-bit master parallel output
22 from a first master data source and a second input channel

23 coupled to said N-bit slave parallel output; and
24 a serialization circuit having an input coupled to
25 an output of said source selection circuit capable of
26 receiving a selected one of said N-bit master parallel output
27 and said N-bit slave parallel output and a serial output,
28 wherein said serialization circuit sequentially shifts out
29 each bit of said selected one of said N-bit master parallel
30 output and said N-bit slave parallel output to produce an
31 output serial data stream; and
32 a digital signal processor capable of receiving and
33 processing said output serial data stream.

1 11. The radio frequency receiver as set forth in Claim 10
2 wherein each bit in said each N-bit slave data packet stored in
3 said slave buffer becomes available in said N-bit slave parallel
4 output substantially concurrently with storage of said each bit in
5 said slave buffer.

1 12. The radio frequency receiver as set forth in Claim 11
2 wherein said slave buffer is a first-in, first-out (FIFO) device.

1 13. The radio frequency receiver as set forth in Claim 12
2 wherein said slave buffer is a 1xN-bit random access memory (RAM).

1 14. The radio frequency receiver as set forth in Claim 10
2 wherein said slave input interface further comprises a slave
3 control circuit capable of receiving said at least one slave timing
4 signal and generating therefrom at least one storage control signal
5 capable of storing said each of said N-bit slave data packets in
6 said slave buffer.

1 15. The radio frequency receiver as set forth in Claim 10
2 wherein said source selection circuit comprises a first multiplexer
3 having an M-bit output.

1 16. The radio frequency receiver as set forth in Claim 15
2 wherein said serialization circuit comprises a second multiplexer
3 having a first M-bit input channel coupled to said M-bit output of
4 said first multiplexer.

1 17. The radio frequency receiver as set forth in Claim 16
2 wherein said serialization circuit comprises a flip-flop circuit
3 having an M-bit input coupled to an M-bit output of said second
4 multiplexer, wherein said flip-flop latches M-bits of data received
5 from said second multiplexer on an M-bit output of said flip-flop.

1 18. The radio frequency receiver as set forth in Claim 17
2 wherein said second multiplexer further comprises a second M-bit
3 input channel coupled to said M-bit output of said flip-flop.

1 19. A radio frequency (RF) transmitter comprising:

2 a serial stream interface capable of receiving a
3 plurality of baseband serial data streams from a plurality of
4 baseband data sources and combining a master serial data stream
5 comprising a sequence of N-bit master data packets and a slave
6 serial data stream comprising a sequence of N-bit slave data
7 packets, said serial stream interface comprising:

8 a slave input interface comprising a slave buffer
9 having a serial input for receiving said slave serial data
10 stream and an N-bit slave parallel output for outputting each
11 of said N-bit slave data packets, wherein said slave buffer
12 stores said each N-bit slave data packet using at least one
13 slave timing signal associated with said slave serial data
14 stream;

15 a source selection circuit having a first input
16 channel capable of receiving an N-bit master parallel output
17 from a first master data source and a second input channel
18 coupled to said N-bit slave parallel output; and

19 a serialization circuit having an input coupled to
20 an output of said source selection circuit capable of
21 receiving a selected one of said N-bit master parallel output
22 and said N-bit slave parallel output and a serial output,

23 wherein said serialization circuit sequentially shifts out
24 each bit of said selected one of said N-bit master parallel
25 output and said N-bit slave parallel output to produce an
26 output serial data stream;

27 a digital signal processor capable of receiving and
28 processing said output serial data stream; and

29 a RF modulation circuit capable of receiving a processed
30 output data stream from said digital signal processor and up-
31 converting said output processed data stream to produce a modulated
32 RF signal.

1 20. The radio frequency transmitter as set forth in Claim 19
2 wherein each bit in said each N-bit slave data packet stored in
3 said slave buffer becomes available in said N-bit slave parallel
4 output substantially concurrently with storage of said each bit in
5 said slave buffer.

1 21. The radio frequency transmitter as set forth in Claim 20
2 wherein said slave buffer is a first-in, first-out (FIFO) device.

1 22. The radio frequency transmitter as set forth in Claim 21
2 wherein said slave buffer is a 1xN-bit random access memory (RAM).

1 23. The radio frequency transmitter as set forth in Claim 19
2 wherein said slave input interface further comprises a slave
3 control circuit capable of receiving said at least one slave timing
4 signal and generating therefrom at least one storage control signal
5 capable of storing said each of said N-bit slave data packets in
6 said slave buffer.

1 24. The radio frequency transmitter as set forth in Claim 19
2 wherein said source selection circuit comprises a first multiplexer
3 having an M-bit output.

1 25. The radio frequency transmitter as set forth in Claim 24
2 wherein said serialization circuit comprises a second multiplexer
3 having a first M-bit input channel coupled to said M-bit output of
4 said first multiplexer.

1 26. The radio frequency transmitter as set forth in Claim 25
2 wherein said serialization circuit comprises a flip-flop circuit
3 having an M-bit input coupled to an M-bit output of said second
4 multiplexer, wherein said flip-flop latches M-bits of data received
5 from said second multiplexer on an M-bit output of said flip-flop.

1 27. The radio frequency transmitter as set forth in Claim 26
2 wherein said second multiplexer further comprises a second M-bit
3 input channel coupled to said M-bit output of said flip-flop.